



■ **Features**

- Fixed 1/4 duty mode, Up to 160 dots.
- Low power consumption design, 6uA current at typical condition.
- Built-in OSC Circuit
- Internal LCD Contrast control Circuit
- Integrated Power-on Reset Circuit
- No external component required
- Interface: 2 wire serial interface
- Compatible with TTL/CMOS
- High EMC immunity

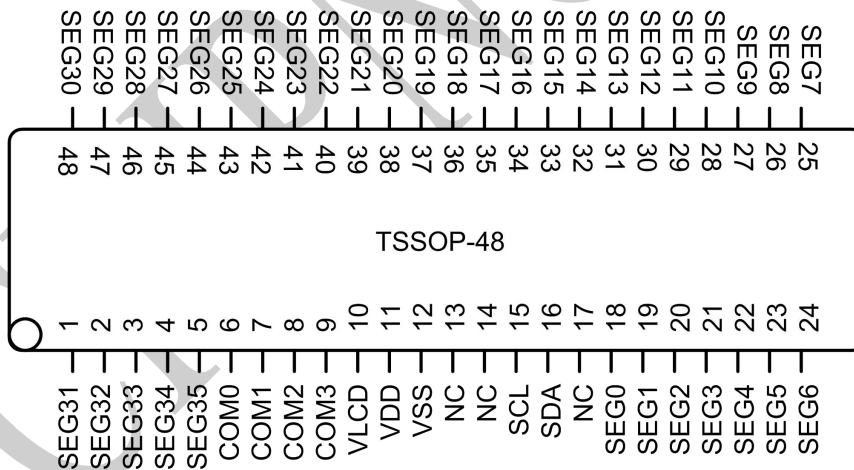
■ **Applications**

- Home electrical appliance
- Meter equipment etc.
- Toys
- PDA
- Clocks

■ **Order Information**

Part No.	Package Type	Tape/Reel
CN90C4S40	TSSOP-48	2500/Reel

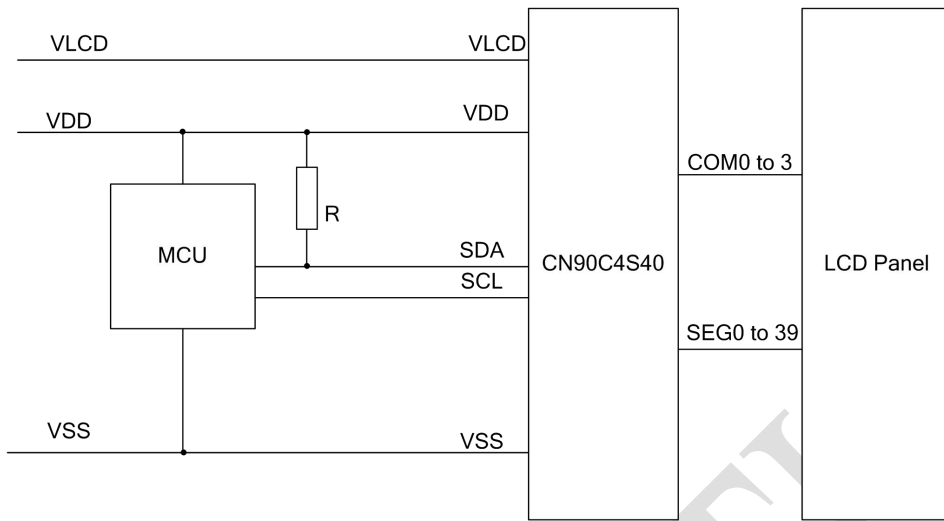
■ **Pin Description**



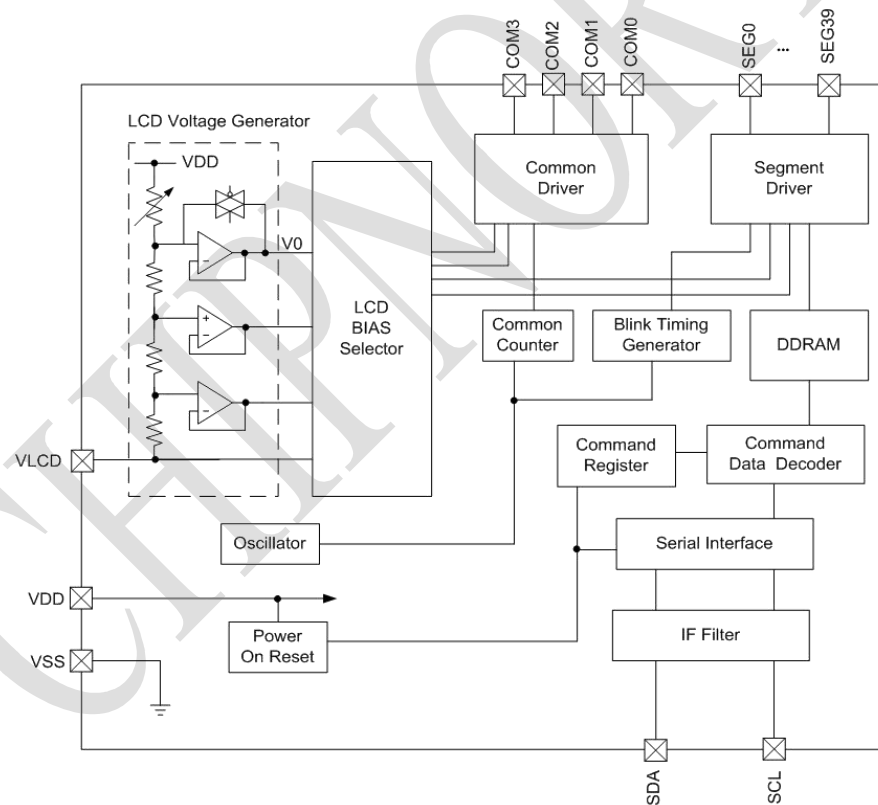
Name	I/O		Function
SDA	I/O	16	2-line serial data input and output
SCL	I	15	2-line serial clock input
VSS	I	12	GND
VDD	I	11	Power supply for logic
VLCD	I	10	LCD biasing voltage, default tie low.
SEG 0~35	O	18~24,25~48,1~5	SEGMENT driver output for LCD
COM 0~3	O	6~9	COMMON driver output for LCD



■ Typical Application Circuit



■ Block Diagram





■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Remarks
VDD Voltage	V _{DD}	-0.5 to + 6	V	Power supply
VLCD Voltage	V _{LCD}	-0.5 to + 6	V	LCD drive voltage
Input voltage range	V _{IN}	-0.5 to VDD + 0.5	V	
Operational temperature range	T _{opr}	-40 to + 85	°C	
Storage temperature range	T _{stg}	-55 to + 125	°C	

■ Electrical Characteristics

Test conditions: VDD=3.3V, TA = 25 °C unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
VDD Power Range	VDD	2.7	-	5.5		
VLCD Power Range	VLCD	2.7	-	5.5	V	LCD drive voltage
"H" Level Input Voltage	V _{IH}	0.7* VDD	-	VDD	V	
"L" Level Input Voltage	V _{IL}	VSS	-	0.3*VDD	V	
SDA "L" Level Output Voltage	VOL_sda	0	-	0.4	V	Iload=-3mA
Frame Frequency	Fclk	-	80	-	Hz	FR=80Hz setting
Standby Current	IDD1	-	-	1	uA	Display off, Oscillation off
Operating Current	IDD2	-	6	20	uA	VDD=3.3V, Ta=25, SR=00, FR=00, Frame inversion, FR=80Hz, with an LCD panel load.

■ Command Registers Description

	7	6	5	4	3	2	1	0
ADSET	C	0	0	P[4:0]				
DISCTL	C	0	1	FR[1:0]		LF	SR[1:0]	
MODSET	C	1	0	ULP	EN	/	/	/
EVRSET	C	1	1	0	0	EV[3:0]		
ICSET	C	1	1	0	1	P[5]	RST	/
BLKCTL	C	1	1	1	0	BF[2:0]		
APCTL	C	1	1	1	1	EV[4]	AON	AOF



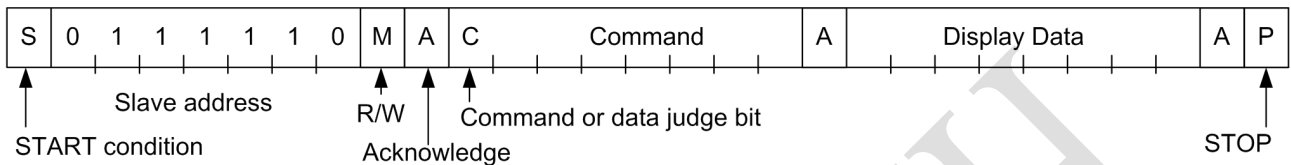
Name	Default	Description
P[5:0]	00000	DDRAM Address. In the write mode, the range of address P [5:0] can be set as 0~2B(Hex). In the read mode, the range of address P [5:0] can be set as 0~2E(Hex). Don't specify another address; otherwise address will be set to "000000". Note: The bit P[5] is in the command 'ICSET'.
FR[1:0]	00	Set Frame Frequency for Power Saving. 00, 80Hz, Normal Mode 01, 130Hz Power Save Mode1 10, 64Hz, Power Save Mode2 11, 200Hz, Power Save Mode3
LF	0	Set Line or Frame inverse mode. 0, Line inverse 1, Frame inverse
SR[1:0]	10	Set internal bias current for Power Saving. 00, *0.5 01, *0.67 10, *1.0, default value. 11, *1.8
ULP	0	Set '1' to enable the Ultra-Low-Power mode, which can decrease total power consumption further more along with 'SR' and 'FR' Power Save Mode.
EN	0	0: disable all blocks on-chip, all com/seg pin will be pulled to GND. 1: enable
EV[4:0]	00000	Adjust resistor divider for LCD contrast setting. 0000, 1.000 * (VDD-VLCD) 0001, 0.975 * (VDD-VLCD) 0010, 0.950 * (VDD-VLCD) 0011, 0.925 * (VDD-VLCD) 0100, 0.900 * (VDD-VLCD) 0101, 0.875 * (VDD-VLCD) 0110, 0.850 * (VDD-VLCD) 0111, 0.825 * (VDD-VLCD) 1000, 0.800 * (VDD-VLCD) 1001, 0.775 * (VDD-VLCD) 1010, 0.750 * (VDD-VLCD) 1011, 0.725 * (VDD-VLCD) 1100, 0.700 * (VDD-VLCD) 1101, 0.675 * (VDD-VLCD) 1110, 0.650 * (VDD-VLCD) 1111, 0.625 * (VDD-VLCD) Note: The bit EV[4] is in the command 'APCTL'.
RST	0	Set '1' to reset all the registers in this table, but it won't reset the display data in the DDRAM.
BF[2:0]	000	Config the blink frequency: 000, No blink. 001, 0.3Hz 010, 0.25Hz 011, 2Hz 100~111, 1Hz
AON: AOFF	00	Config the pixel display 00, All pixels are ON/OFF depending on the data in the display DDRAM. 01, All pixels are OFF regardless of DDRAM data. 10, All pixels are ON regardless of DDRAM data. 11, All pixels are OFF regardless of DDRAM data, the same as '01'.



■ Function Description

● Command and Data Transfer Method

1. Generate "START condition".
2. Issue Slave address 7C.
3. Transfer command.
4. Transfer display data.
5. Generate "STOP condition"



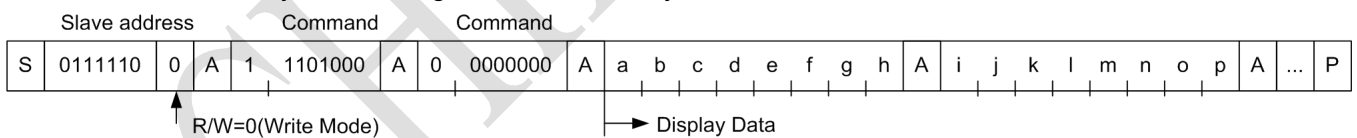
● Write Display Data and Transfer Method

Set R/W bit to '0' to come into write mode.

This device has Display Data RAM (DDRAM) of 40×4=160 bit.

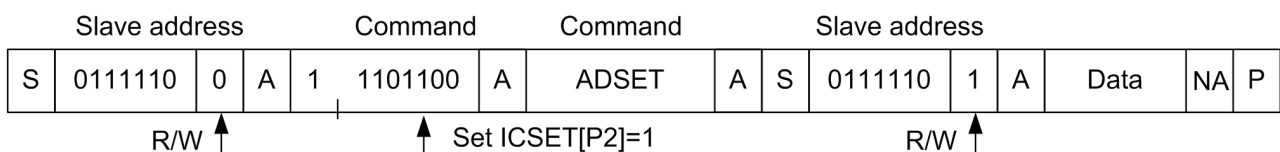
		DDRAM address													
		00	01	02	03	04	05	06	07	25H	26H	27H		
BIT	0	a	e	i	m									COM0	
	1	b	f	j	n									COM1	
	2	c	g	k	o									COM2	
	3	d	h	l	p									COM3	
		SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG37	SEG38	SEG39		

8-bit data will be stored in DDRAM. The address to be written is the address specified by Address set command, and the address is automatically incremented in every 4bit data. Data can be continuously written in DDRAM by transmitting Data continuously.



● Read Command Register and Transfer Method

The command registers can be read during read mode. The sequence for the command registers reading is shown below and is similar to the display data reading sequence.



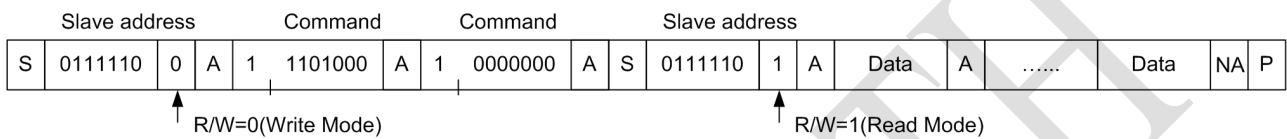


The command register addresses are described below. The following register settings can be read in this mode.

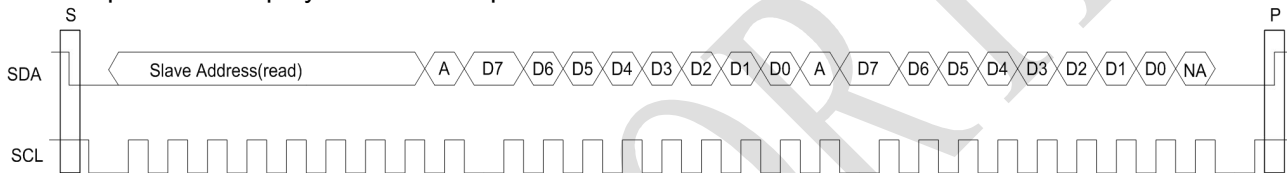
Register	D7	D6	D5	D4	D3	D2	D1	D0	Address
REG1	/	/	/	/	RST	BF[2:0]			2CH
REG2	FR[1:0]		SR[1:0]		LF	EN	AON	AOF	2DH
REG3	/	/	/	ULP	EV[3:0]			2EH	

● Read Display Data and Transfer Method

The read mode sequence is shown below

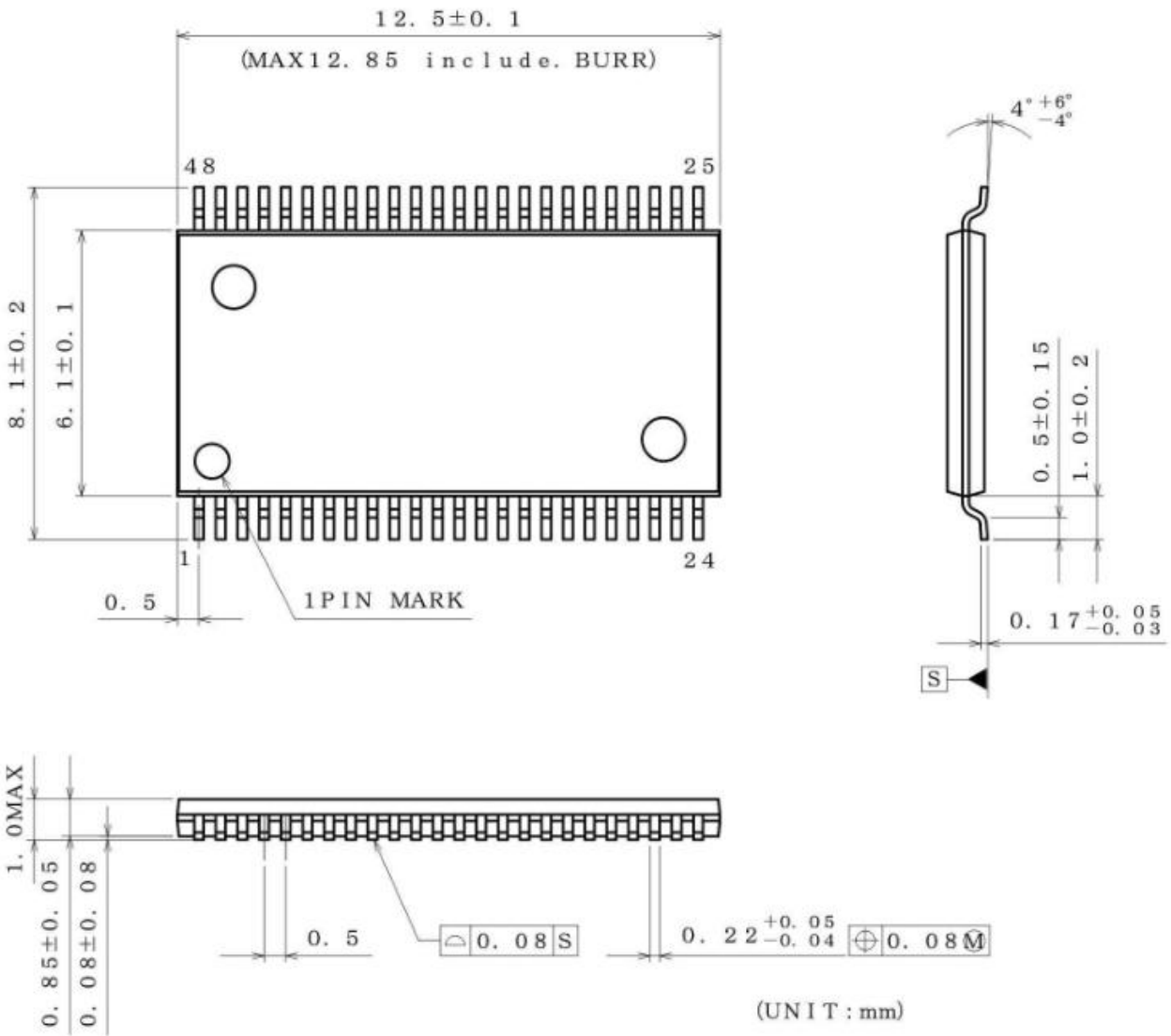


An example of the display data read sequence is shown below.





■ TSSOP48 Package





■ ORDER INFORMATION:

date	Version	Revision notes	Reviser
2020.3.19	V1.0	Initial data compilation	ZhangSongfeng

CHIPNORTH